[Hari* *et al.*, 5.(5): May, 2016]
IC™ Value: 3.00

ISSN: 2277-9655
Impact Factor: 3.785

IJESRT

INTERNATIONAL JOURNAL OF ENGINEERING SCIENCES & RESEARCH TECHNOLOGY

SIMULATION OF MODIFIED AGC AND PRE—SYNCHRONIZATION PROCESSOR IN LOW POWER SOFTWARE DEFINED RADIO RECEIVER

Hari Hara P Kumar M
Research Scholar, Electronics and Communication Engineering, Sri Satya Sai University of Technology and Medical Sciences, Sehore, India

DOI: 10.5281/zenodo.51905

ABSTRACT

In this paper, we can conclude that there is a reduction of power consumption by modifying the existing system of software define radio receiver (SDR). From the existing module, the digital front end architecture of SDR contains the two processors known as AGC (Automatic Gain Controller) processor and pre synchronization processors to perform the signal detection and pre synchronization operations. The AGC is used to optimize the ADC range based on the analog front end control things. After the AGC detection, the synchronization operation is done by an application specific processor. In this system, when the sync signal is asserted the digital front end power management can disable the synchronization process and wakeup base band part of the SDR. In the proposed system, the AGC controller and pre synchronization engine processors are integrated into a single processor with different ALUs working for AGC and pre synchronization operations. An ASIC code for detection and synchronization is executed using VLIW processor operation and power management is performed. When AGC is on, the pre synchronization ALU and remaining parts are off. When AGC is completed, the pre synchronization processor is on and AGC is power down. At the end an interrupt is generated to wake up the base band processor. With this, the energy scalable design is achievable and the low power implementation is to be done.

KEYWORDS: SDR, Automatic Gain Controller (AGC), Pre—synchronization, VLIW processor, ADC.

INTRODUCTION

The SDR platform template is depicted in Figure 1. It is specifically designed to support SDR implementation of IEEE 802.11n WLAN and IEEE 802.16e mobile wireless broadband access. A RISC platform controller is considered and is responsible for the MAC functionality and the PHY processing macro-pipeline scheduling. This core is coupled through a multi-layer AHB bus to three types of processing units: digital front-end (DFE) tiles, baseband modem engines and forward error correction (FEC) engines, signal detection, decimation, burst pre-synchronization (in receive mode) and signal interpolation (in transmit mode).

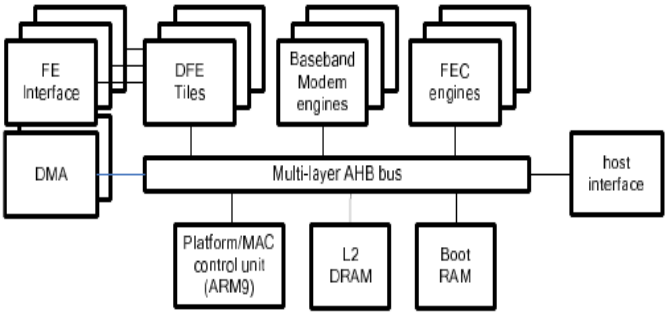

Figure 1 Top level view of the SDR platform template

ISSN: 2277-9655
Impact Factor: 3.785

To support multi-antenna operations, three DFE tiles are coupled with three analog front-end signal paths. Each class of processing units has a different programmability/ performance/energy-efficiency tradeoff. For the baseband processors, programming productivity and performance are the main concerns. Energy-efficiency may be slightly relaxed because of the lower duty cycle and the possible energy-scalable implementation of the supported functions. Digital front-end units however require a more balanced tradeoff between programmability (to be able to detect burst from different standards) and energy efficiency (as they are almost continuously active and, hence, are the main contributors to the standby power). Such opportunistic partitioning, when combined with aggressive power management, is extremely valuable when implementing burst-based communication standards.

DFE ARCHITECTURE

From the figure 2, the DFE consists of multiple 'tiles'. A single tile contains the digital receive and transmit logic to interface to a single antenna. The transmitter part of a DFE tile consists of a buffer and a VLSI interpolation filter. The interpolation filter is based on an optimized implementation of a 19-taps half-band filter (with hamming window) for a fixed up sampling of factor two. A start command can be issued allowing the samples to be clocked out towards the analog front-end through the filters. The transmit (TX) buffers have a programmable threshold that triggers an interrupt once the number of available samples falls below this threshold. This interrupt is handled by the platform controller.

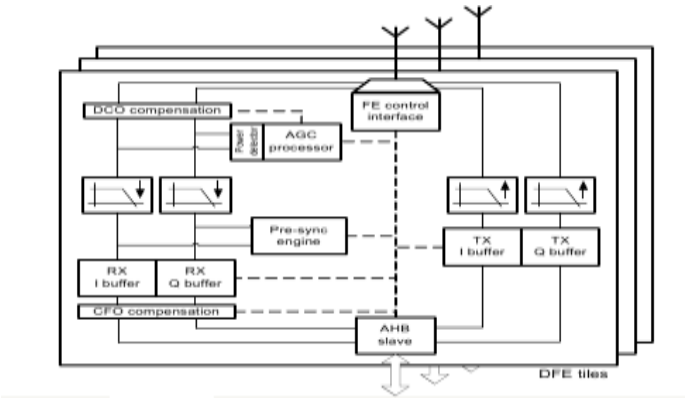

Figure 2 Digital Front end architecture

The receiver part of a DFE tile contains a chain made of the VLSI decimation filters, the buffers and compensation units for DC offset and carrier frequency offset (CFO). The decimation filter impulse response is derived from a 19-taps half-band filter with hamming window performing a energy efficient factor two down sampling. Next to the data path, two dedicated micro-processor cores are implemented. The first microprocessor handles the front-end automatic gain control (AGC) and the DFE power management. The second one is optimized for time synchronization.

LITERATURE REVIEW

AGC CONTROLLER ARCHITECTURE

A power detection unit with variable delay line of 8 or 32 samples determines the received signal power and is capable of DC offset estimation. A dedicated microcontroller is used to implement the AGC algorithm that removes DC offset and optimizes the ADC range based on the analog front-end control pins. The controller also determines which other parts of the DFE RX are activated after an AGC event is detected (gradual wakeup). The controller architecture is depicted in Figure 3, it is clocked at the sample rate (40MHz). It has an instruction memory of 512 14-bit words and a data scratchpad of 32 8-bit words, both implemented as register file macros. The instruction set and the architecture of the controller are compatible with an industry-standard Microchip PIC16F84.This allows for reuse of the available tool chains, including c-compilers and debuggers.

ISSN: 2277-9655
Impact Factor: 3.785

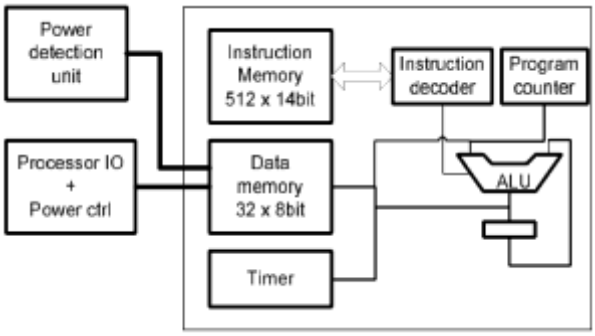

Figure 3 AGC Controller Architecture

PRE—SYNCRONIZATION PROCESSOR

As soon as the AGC controller detects the presence of a potential signal and has optimized the ADC range accordingly, a dedicated application specific processor (ASIP) is activated to perform time synchronization. The ASIP has 2-issue VLIW architecture shown in Figure 4. The first slot is made of a 16-bit data path for address computation and control. The second slot is a 128 bit vector unit. The processor also contains a vector scratchpad of 32kbit (256x128bit) and an instruction memory of 20kbit (512x40bit). The synchronization algorithm is executed as follows. A data vector is fetched from the ASIP scratchpad, which always contain a copy of the main data path FIFO content. Next, the correlation and the input signal power are calculated. In the case of the 16e mode, this includes keeping track of a set of moving sums. However,for both modes we determine the running maximum of the correlation with respect to the input signal power. Whenever a correlation peak above a defined threshold is detected, the computation stops, the index of the maximum is written to an output port and the sync signal is asserted. The sync signal is then interpreted by the DFE power management processor, which in turn disables the synchronization processor and wakes up the baseband part of the platform so that the received data can be transferred for processing. For real time 802.11a/g/n synchronization, the processor has to run at minimum 130 MHz. The 802.16e mode requires a clock rate of 280 MHz.. The ASIP clock is set to 140MHz or 280MHz depending on the mode. In case of 140MHz operation, voltage can be reduced from 1V to 0.8V.

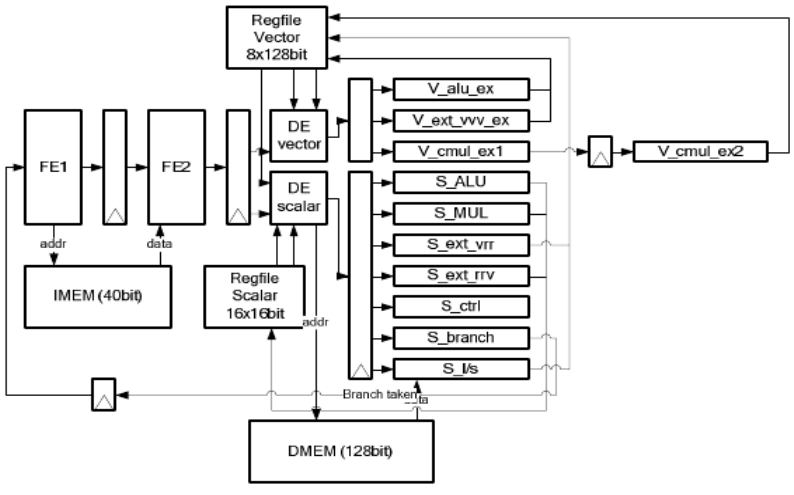

Figure 4 Pre—Syncronization Architecture

ISSN: 2277-9655
Impact Factor: 3.785

WORKING PRINCIPLE

SIGNAL DETECTION AND PRE-SYNCHRONIZATION PROCESS

For data transmission, the TX buffers and interpolation filters are powered up. An 'almost empty' threshold is programmed in the transmit buffer block, allowing an interrupt driven loading method of the buffers. Once a start command is sent to the transmit buffers, samples are clocked out of the buffers, filtered, and sent towards the analog front end. At the end of the burst, the transmit buffers and interpolation filters are put back in sleep mode. A burst reception through the RX part of a DFE tile is organized as follows. When the receive part is activated, only the AGC controller is powered. The front end is programmed with its initial settings. When the receive threshold power is reached, the controller performs the AGC algorithm, and a fine DC offset estimation is performed. The DC offset is fed back to the compensation unit. At the same time, the receive filters; the sample buffer and the synchronization ASIP are activated. Once the ASIP detects a packet preamble, the sample index at which synchronization was reached is stored and the ASIP is powered down.

The synchronization point is then adapted by a programmable offset to determine the first sample of the burst that will be transferred towards the baseband processor. The platform controller is notified of the synchronization event by the DFE microcontrollers asserting a plat form level interrupt. During the wake-up time of the baseband processor, samples are stored in the DFE RX buffers. These buffers have a programmable threshold level, which again enables event driven buffer readout. At the end of the burst, the complete receive path, except for the AGC and power detection unit, is powered down and a new burst detection can take place. In case of a blocker signal, AGC is performed but no synchronization event occurs. After a time out counted down by the AGC controller timer, the buffers are flushed and turned off; the filters and synchronization ASIP are deactivated. Finally, the data path of the RX DFE is augmented with a carrier frequency offset (CFO) compensation unit that is capable of performing a rotation on the time domain signal. The settings of that block are programmable through the AHB bus interface. The CFO value is programmed to be the measured value of the previous burst and can be updated during the reception burst if required. At the end of the burst, the complete receive path, except for the AGC and the power detection unit, is powered down and a new burst detection can take place.

ACTIVITIES OCCUR WHEN DETECTING A VALID SIGNAL

To guarantee detect ability of a potentially incoming burst, only the AGC controller and power detector data path must be activated. The other components are completely switched off by means of power gating. However, to guarantee seamless start up, the instruction memory of the synchronization processor must be kept supplied. Using substrate biased SRAM, one can still significantly reduce the leakage. Hence, the minimum power for detect ability is the sum of, on the one hand, the AGC active and static power, its memories and, on the other hand, the leakage power of the synchronization processor program memory when set in retention sleep mode. The sequence of operations required guaranteeing the detection and pre-synchronization of a valid burst (802.11a case) is illustrated in Figure 5. The AGC enable signal is high when the DFE tile is active. The AGC controller is continuously analyzing the incoming data. Power detection is signaled by AGC done (on time index 18025ns in our simulation). This yields the assertion of the sync_enable, filter enable and buffer enable signals that activate respectively the synchronization processor, the decimation filters and the data FIFO. Considered an input signal, a synchronization event occurs at time index 27675 (sync) signal from the Figure 5. This causes the assertion of a platform level interrupt (DFE int), which wakes up the platform controller. The power state flow is appended to Figure 7, Summing up the state power multiplied by the state duration, one can easily compute the energy consumed during the burst detection. Specifically, we consider the energy spent between the receptions of the first valid sample until the generation of the DFE interrupt. In the current experiment, this gives 228nJ.

ISSN: 2277-9655
Impact Factor: 3.785

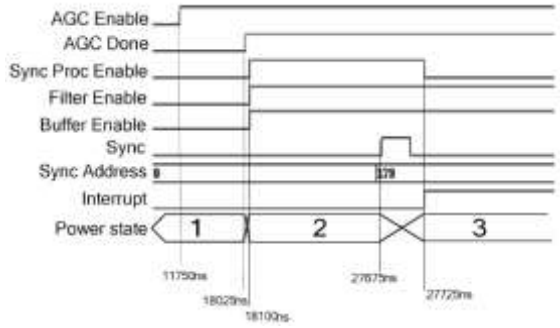

Figure 5 Activity trace when detecting a valid burst.

ACTIVITIES OCCUR WHEN DETECTING A FALSE SIGNAL

Similarly, the sequence of operation occurring at the reception of a blocker signal (false trigger) is depicted in Figure 6. Although an AGC done signal is generated and the filter, buffer and synchronization processor are activated, no synchronization point is found and hence, the 'sync' signal is not asserted. Filter, buffer and synchronization processor are forced back to sleep mode after a time-out occurs at time index 31025ns.

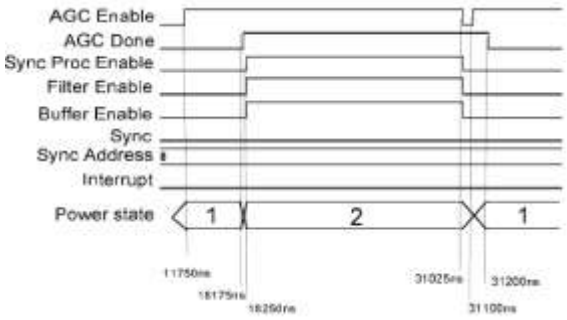

Figure 6 Activity trace when detecting a false signal

POWER STATE MACHINE

In this section, we focus on the function blocks required in reception mode. In transmit mode, the contribution of the DFE can be neglected compared to the rest of the SDR SOC. The power consumption of the AGC controller with its power measurement line, its IMEM and DMEM, the decimation filter and the detection and synchronization ASIP (with IMEM and DMEM) has been evaluated using Synopsys Prime Power TM. Power simulation is done at gate level for each entity separately with test vectors corresponding to the execution of their respective code detection, synchronization and buffering. The bus interface is not considered in our experiment. The static and dynamic power consumption of the different components are summarized in Table 1. Based on this data and considering the different combination of active component together with the possible transitions, the system power state machine can be derived Transition times are further investigated. In the following, the power state machine is used in order to evaluate the average power needed to guarantee detection of a burst (detectability) and the energy spent in the detection and pre-synchronization of a valid signal or the detection and reject of a blocker signal

ISSN: 2277-9655
Impact Factor: 3.785

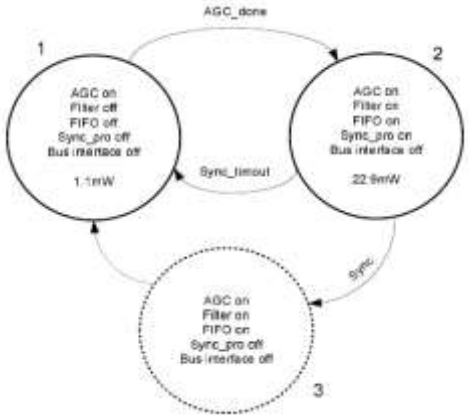

Figure 7 Power state machine

Table 1 DFE RX component power consumption

Component	Active (mW)	Static (αW)	Sdby (αW)
AGC datapath	.40	2	-
AGC Controller	.13	.7	-
AGC IMEM	.20	2	1
AGC DMEM	.34	3	-
Decimation Filter	.86	4	-
FIFO buffer	2.74	27	-
Sync ASIP core	14.27	71	-
Sync ASIP IMEM	2.47	25	12
Sync ASIP DMEM	1.37	13	-

ISSN: 2277-9655
Impact Factor: 3.785

PROPOSED SYSTEM

In the proposed system, the AGC controller and pre synchronization engine processors are integrated into a single processor with different ALUs working for AGC and pre synchronization operations as shown in figure 8. An ASIC code for detection and synchronization is executed using VLIW processor operation and power management is performed. When AGC is on the pre synchronization ALU and remaining parts are off. When AGC is completed the pre synchronization processor is on and AGC is power down. At the end an interrupt is generated to wakeup the base band processor. With this the energy scalable design is achievable and the low power implementation is done.In this paper the behavior of the system was described in a Hardware description language (VHDL), which can be synthesized into a structural description. After simulation verifies proper operation, the design will be placed and routed using technology dependent tools like FPGA.

Modified AGC and Pre-synchronization Architecture

In the proposed system as shown in Figure 8, a VLIW processor is designed which contains automatic gain controller and pre synchronization processor. With this the digital front end architecture become simple and the VLIW operation can give low power consumption along with the synchronization operation. In this processor we are using an AGC ALU and a Vector ALU. The system has the flexibility that when AGC ALU on, the vector ALU is off and vice versa. With this architecture power can be saved. All the instructions used for synchronization operation in the existing system are executed in the proposed system also. And the power management along with pre synchronization can be achieved. This processor is implemented in VHDL and can be downloaded into FPGA.

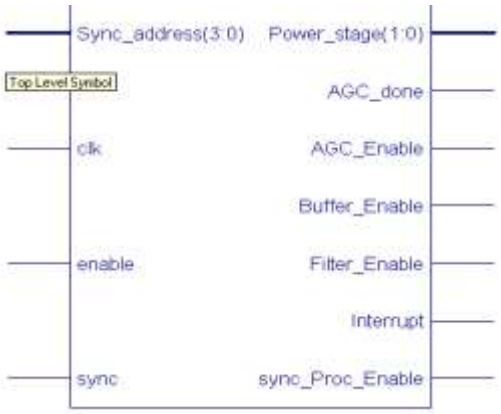

Figure 8 Block diagram of Modified AGC and Pre-synchronization Architecture

In this system, when a burst signal came from the transmitter buffer, an AGC enable first given to processor. Now the AGC ALU is powered and when a threshold power is reached it can perform competition and we can give an AGC done. At the same time the synchronization ALU is activated and the routine given above is executed. The synchronization pulse is then adapted by the processor to determine the first sample of reception. After this sync pulse, an interrupt is generated and the sample will be transferred to the base band processor. During the wake up of the base band processors a new power level can be taken. And the system is ready for a new detection when the AGC is again power. In the case of a false or blocker signal AGC is performed but no synchronization pulse is generated. After certain time the synchronization ALU is disabled and again the processor goes to first power state with AGC on and synchronization off. Thus these proposed processors can perform power detection and pre synchronization.

SIMULATION RESULTS

The proposed architecture is integrated simulated by using model sim 5.5e.The simulation results show that the interrupt can be generated only when a valid signal is detected.

ISSN: 2277-9655
Impact Factor: 3.785

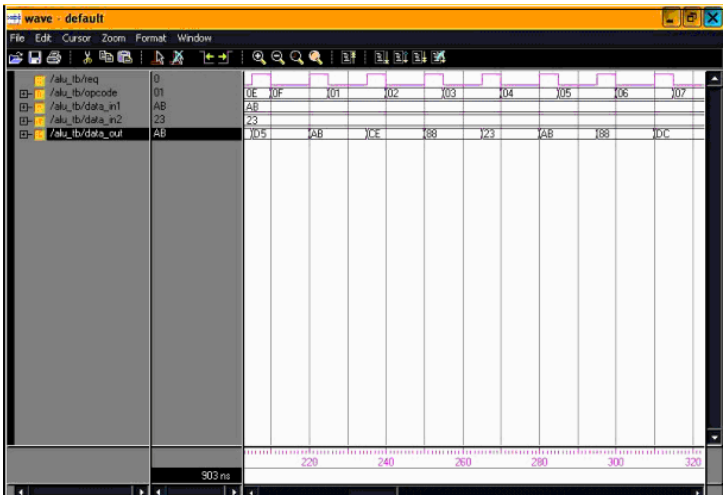

Figure 9(a)

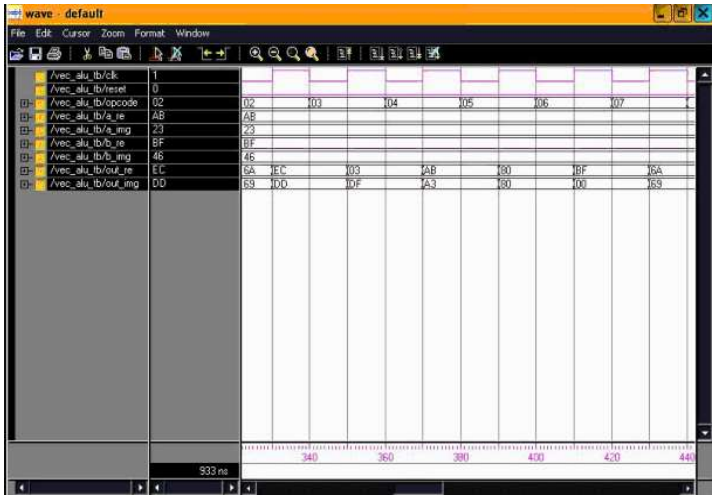

Figure 9(b)

Figure 9 (a) and (b) shows Simulation of ALUand vector ALUrespectively

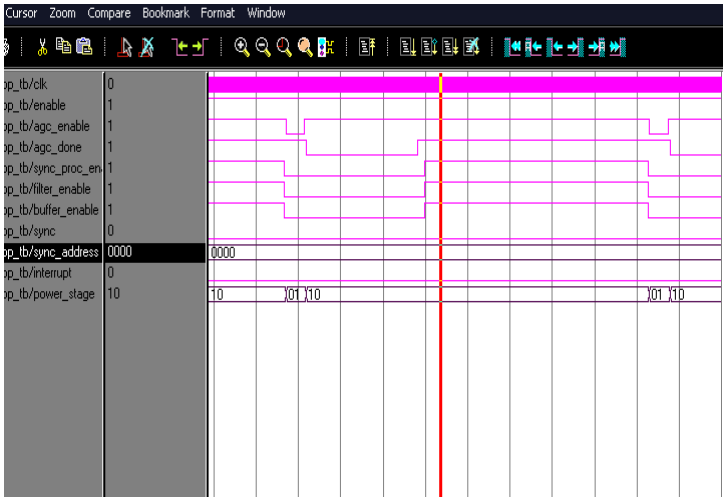

Figure 10 (a)

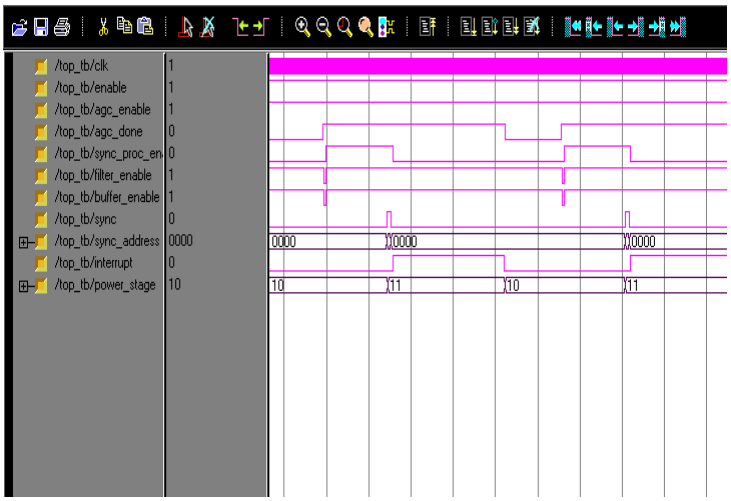

Figure 10 (b)

Figure 10 (a) shows the simulation result of the proposed system, when a false signal is detected and Figure 10 (b) shows the simulation result of the proposed system, when a valid signal is detected

SYNTHESIS REPORT
POWER CONSUMPTION REPORT
Release 9.2i - XPower SoftwareVersion:J.36

Design: top.ncd

ISSN: 2277-9655
Impact Factor: 3.785

Preferences: top.pcf

Part: 3s500epq208-4

Data version: ADVANCED, v1.0, 10-03-13

Power summary:	I (mA)	P (mW)
Total estimated power consumption:	349	
Vccint 1.00V:	18	18
Vccaux 2.50V:	131	328
Vcco25 2.50V:	1	3

Clocks:	0	0
Inputs:	0	0
Logic:	0	0
Outputs:		
Vcco25:	0	0
Signals:	0	0

Quiescent Vccint 1.00V:	18	18
Quiescent Vccaux 2.50V:	131	328
Quiescent Vcco25 2.50V:	1	3

Thermal summary:

Estimated junction temperature: 28C

Ambient temp: 25C

Case temp: 26C

Theta J-A range: 10 - 36 C/W

Analysis completed: Sat May 7 09:58:58 2016

RTL SCHEMATIC

The below Fig. shows the RTL Schematic of low power modified AGC and pre synchronization processor internal module -1 and module 2.

ISSN: 2277-9655
Impact Factor: 3.785

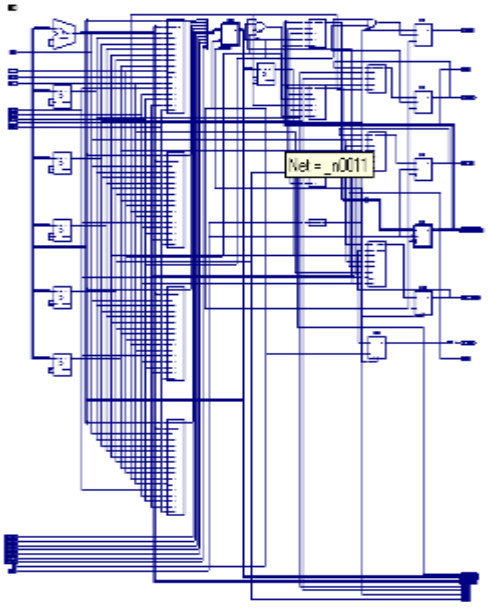

Figure 11 (a)

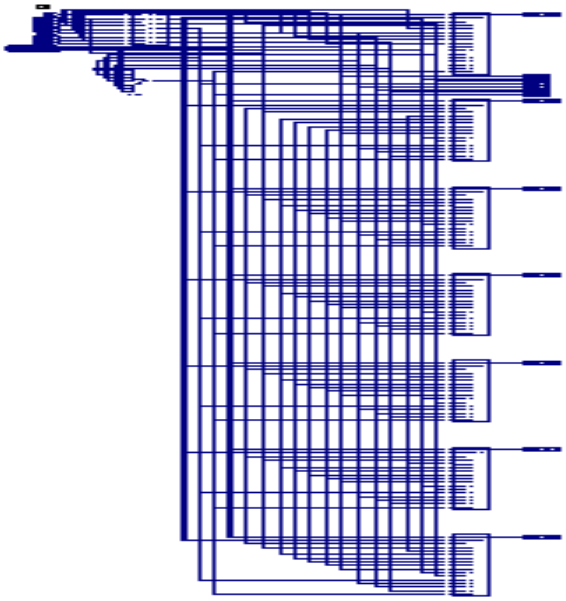

Figure 11 (b)

Figure 11 (a) shows RTL Schematic of low power modified AGC and pre synchronization processor internal module -1
Figure 11 (b) shows RTL Schematic of low power modified AGC and pre synchronization processor internal module -2.

CONCLUSUION

In this paper, a new processor architecture for low power detection and pre synchronization. This design approach can also be applied for remaining blocks of digital front end. The AGC ALU is designed and simulated. The pre synchronization ALU performs vector operations and the ASIP code is executed. These two ALU are placed in the modify architecture and simulated. The power state machine operation is also done and shown in the simulated output. It can employ low power consumption. This proposed architecture has been verified by simulation at the model level and currently the system has been integrated and is being tested by using test bench. The design is synthesized and the report is shown.

REFERENCES

[1] Abe,M., Sasho,N,.Morelos-Zaragoza,R,.and Haruyama,S,.(2001) "An RFArchitecture for Software Defined Recivers", Microwave Workshop & Exhibition 2002, Yokohama.
[2] Bose,V. and Ismert,M., Welborn,M. and Guttag,J. (1999) "Virtual radios," IEEE Journal on Selected Areas of Communications", vol. 17
[3] Deslandes,D. and Wu,K,.(2001) "Integrated microstrip and rectangular waveguide in planar form," IEEE Microw. Guided Wave Lett., vol. 11,no. 2.
[4] Hesselbarth,J. and Wiedmann,F. and Huyart,B. (1997) "Two New Six-Port Covering Very Large Bandwidths", IEEE Trans. on Instrumentation and Measurement, vol. 46, no.4.
[5] Mitola, J. (1995) "The software radio architecture," IEEE Commun. Mag.,
[6] O. Tatu,S,.Moldovan,E,. Wu,K,.and G. Bosisio,R,.(2001) "A new direct millimeter-wave six-port receiver," IEEE Trans Microw. Theory Tech., vol. 49, no. 12.
[7] Tennenhouse, D.L and Bose,V.G. (1996) "The spectrumware approach to wireless signal processing," Wireless Networks, vol. 2, issue 1
[8] Tuttlebee, W. (1997) "The impact of software radio," Presented at the Software Radio Workshop", Brussels, Belgium.
[9] Xu,X,. and G. Bosisio,R. and Wu,K.(2005) "A new six-port junction based on substrate integrated waveguide technology," IEEE Trans Microw. Theory Tech., vol. 53, no. 7.